E. Remarks

Rejection of Claims 9, 11 and 12 Under 35 U.S.C. §102(b) based on *Furutani* (U.S. Patent No. 5,673,231).

The invention of amended claim 9 is directed to a method of reducing a standby current contribution in conductive lines of a memory device. The method includes providing at least one transistor between each of a plurality of conductive lines arranged in a first direction within a memory cell array and a corresponding circuit coupled to the conductive line. Such a step includes providing at least one transistor between a bitline and a corresponding sense amplifier circuit. In addition, a fuse-type element is programmed to generate a control signal first value if an associated conductive line is determined to have a defect. The method further includes disabling each transistor when the associated control signal has the first value to prevent defect induced current from flowing through the transistor with respect to the corresponding conductive line.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference.

The cited reference *Furutani* is not believed to show or suggest programming a fuse-type element to "generate a control signal first value if an associated conductive line is determined to have a defect" and "disabling each transistor when the associated control signal has the first value".

Furutani discloses a semiconductor memory device in which leakage current from a memory cell can be suppressed during a standby mode. As shown in FIG. 1 of *Furutani*, the cited reference teaches a memory cell array in which transistor pairs (19/20 and 21/22) connect bit line pairs to a common differential amplifier (5). The operation of transistor pairs 19/20 and 21/22 can be controlled, in part, by the state of two fusible links 9/10 and 11/12 corresponding the each bit line pair.

However, the description of *Furutani* appears to describe an operation that is essentially the opposite of Applicants' claim 9. As emphasized above, in Applicants' claim 9, for a conductive line determined to have a defect, a fuse-type element is programmed to result in the disabling of transistors provided between the bit lines and a corresponding circuit. *Furutani*

shows the enabling of transistors when a defect exists.

In more detail, *Furutani* indicates how fuses are set when a defect occurs:

> Next, a case in which there is a failure due to short-circuit between bit line BL0a and word line WL0a and there is no failure due to short-circuit between bit lines BL1a to BL3a as well as bit lines BL1a to BL3a and word line WL0a will be described...
>
> Node N2 is set at the potential of /ϕ2 by ***disconnecting a fuse element 12*** of the column decoder for driving column selecting line Y0 ***which selects bit lines BL0a, BL0a with failure*** due to short-circuit. A node N3 is set at the potential of ϕ2 by ***disconnecting fuse element 9*** of the column decoder for driving column selecting lines Y1 to Y3 ***which selects bit lines BL1a to BL3a and BL1a to BL3a with no failure*** due to short-circuit. (*Furutani*, Col. 9, Lines 32-52, emphasis added).

Thus, in the description that follows, fuse element 12 is disconnected for the bit lines containing the failure. This results in transistors 21/22 being enabled, not disabled, as recited in Applicants' claim 9:

> When a row strobe signal RAS="H" level... since column address activation signal /ϕ2 is at "H" level. Accordingly, column selecting line ***Y0 attains "H" level.*** Thus, since P channel MOS transistor 32 is rendered non-conductive, there is no leakage current flowing to word line WL0a from interconnection 50 supplying $V_{CC}/2$ potential even when there is a failure due to short-circuit between bit line BL0a and word line WL0a. (*Furutani*, Col. 9, Lines, emphasis added).

As can be understood from FIG. 1 of *Furutani*, when "Y0 attains 'H' level" transistors 21/22 are enabled.

Accordingly, because the reference shows the enabling of transistors for those lines with a failure, the reference is believed to teach away from Applicants' amended claim 9 limitations.

Rejection of Claims 9 and 10 Under 35 U.S.C. §102(b) based on *Yamauchi et al.* (U.S. Patent No. 6,246,627).

Applicants have amended claim 9 to include the limitations of dependent claim 11. Claim 11 was not rejected based on *Yamauchi et al.*[1]. Accordingly, this ground for rejection is believed to be traversed.

Rejection of Claims 9 and 13 Under 35 U.S.C. §102(b) based on *Kawai et al.* (U.S. Patent No. 5,146,429).

As noted above, Applicants have amended claim 9 to include the limitations of dependent claim 11. Claim 11 was not rejected based on *Kawai et al.*[2] Accordingly, this ground for is rejection believed to be traversed.

Claims 9 and 12 have been amended. Claim 12 has been amended to provide correct claim dependency, and not in response to the cited art. Claim 11 has been cancelled.

The present claims 1-10 and 12-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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Bradley T. Sako
Attorney
Reg. No. 37,923

Bradley T. Sako
WALKER & SAKO, LLP
300 South First Street
Suite 235
San Jose, CA 95113
Tel. 1-408-289-5315

[1] See the Office Action, dated 5/10/2005, Page 3, Section 5, which shows only original claims 9 and 10 are rejected based on this reference.

[2] See the Office Action, dated 5/10/2005, Page 4, Section 6, which shows only original claims 9 and 13 are rejected based on this reference.

D. Amendments to Drawings.

A replacement sheet for FIG. 3 is submitted herewith. The label "flatch" has been changed to "latch".